AMENDMENTS TO THE CLAIMS

Please cancel claims 26, 29-39, and 41-44 and without prejudice or disclaimer of their underlying subject matter.

Please amend the claims as follows.

1-26. (Canceled)

27. (Currently amended) ~~A data processing apparatus as set forth in claim 26, further comprising:~~

A data processing apparatus comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data;

a coincidence detecting circuit adapted to compare said ~~program~~ address with said bug address and output ~~said~~ an interrupt request signal, ~~wherein~~ said interrupt request signal indicating ~~es~~ coincidence or non-coincidence of said ~~program~~ address and said bug address;

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

28. (Previously presented) A data processing apparatus as set forth in claim 27, wherein said value is incremented when said interrupt request signal indicates said coincidence.

29-39. (Canceled)

40. (Currently amended) ~~A data processing apparatus as set forth in claim 34~~ A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address,

wherein another program address indicates a location within said program memory for another of the instruction codes, and

wherein said value of the counter register is incremented by 1.

41-44. (Canceled)

Please add the following new claims.

45. (New) A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

46. (New) A data processing apparatus as set forth in claim 45, wherein said counter register is located within a random access memory at a predetermined memory address.

47. (New) A data processing apparatus as set forth in claim 45, further comprising:

bug address setting registers adapted to store said first and second bug addresses.

48. (New) A data processing apparatus as set forth in claim 45, wherein said first bug address indicates a starting address within said program memory for a first buggy part of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program.

49. (New) A data processing apparatus as set forth in claim 48, wherein said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part.

50. (New) A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals.

51. (New) A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.

52. (New) A data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.